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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,358	10/19/2000	Coke S. Reed	M-9051 US	8267

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ART UNIT	PAPER NUMBER
2663	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/693,358	REED ET AL.	
	Examiner	Art Unit	
	Nittaya Juntima	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,11-18,21,26,27,29,37-44,50,51 and 56* is/are rejected.

7)☒ Claim(s) *6-8,10,19-20,22-25,28,30-36,45-49,and 52-55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- on pages 1, 6-9, 13, and 16-18, the United States patent application serial numbers are missing and the corresponding attorney docket numbers should be deleted;

- on pages 4-6, 13, and 18, "patent application serial No. 09/009,703" should be replaced with "Patent number 6,289,021;"

- on page 5, paragraph 4, line 5, "108" should be changed to "106;"

- on page 6, line 2, "100" should be changed to "102;"

- on page 7, paragraph 3, line 2, "302" should be changed to "310;"

- on page 15, line 8, "any" should be changed to "many".

Appropriate correction is required.

Claim Objections

2. Claims 6, 8, 10, 21-25, 29-33, 35-36, 38, 40, 45, 47-48, 53 are objected to because of the following informalities:

- in claim 6, line 7, "routs a" should be changed to "routes the;"

- in claims 8, 10, 22-25, 29-33, 35-36, "HQOS" and "LQOS" should be spelled out as "high quality-of-service" and "low quality-of-service," respectively, to make the claim clearer;

- in claim 21, line 4, "at" after "M" should be deleted;

- in claim 38, line 20, "or" should be added after "one;"

- in claim 40, line 18, "are" should be changed to "is;"
- in claim 45, lines 10 and 11, "B_3" should be changed to "D_3;"
- in claim 47, line 11, "B_3" should be changed to "D_3;"
- in claim 48, lines 6 and 7, "sends" should be changed to "sending" and

  line 12, "B_3" should be changed to "D_3;" and
- in claim 53, lines 6 and 7, "CSI(i)" and "$CSI_0(A,D)$" should be changed to "CS(i)" and "$CS_0(A,D)$," respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 11-14, 27, 29, 37, and **39-40** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3, the limitation "an output port that is reachable from node A and is not reachable from the node D" in line 4-5 of the claim is vague and indefinite. It cannot be determined from the claim language as how an output port is only reachable from the node A and not from the node D when a message can reach the output port through the node D which is closer to the output port as shown in Fig. 1A and indicated in the specification page 4, lines 1-3 from the bottom of the page. The office is treating the limitation as "an output port that is reachable from node A and is not reachable from the node B."

Claim 39, the limitation "control signals C being received by a node of the plurality of nodes at a discrete time step t" in lines 7-8 of the claim is vague and indefinite. It cannot be determined from the claim language as how more than one control signals C can be simultaneously received at time step t as this is not supported by the specification, specifically on page 13, lines 1-6.

Claims 11, line 3, "the message set R" lacks antecedent basis.

Claim 14, line 2, "the message selecting means" lacks antecedent basis.

Claim 27, line 7, "the property" lacks antecedent basis.

Claim 29, lines 3-4, "the message set" lacks antecedent basis.

Claim 37, line 11, "the multiple levels" lacks antecedent basis.

Claim 40, lines 20-21, "the direct message output connections of the node A" lacks antecedent basis.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 42 is rejected under 35 U.S.C. 102(b) as being anticipated by an art of record, Coke S. Reed (WO 97/04399).

Reed teaches an interconnect structure comprising ***a plurality of nodes and a plurality of interconnect lines*** (page 4, lines 21-24), ***the interconnect structure transmitting a plurality of***

multiple-bit messages entering the interconnect structure unsorted through a plurality of input ports (input ports of nodes at level J) (page 5, line 10, page 22, lines 11-12, 15-18, page 31, lines 25-page 32, lines 1-2), ***an individual message M being self-routing*** (having a header designating the target ring in a binary form, page 31, lines 25-page 32, lines 1-2), ***the interconnect structure includes a node E*** (node E) ***having a first data input interconnection from a node A*** (node A) ***and a second data input interconnection from a node F*** (node F) ***distinct from the node A, and a control interconnection between the node A and node F for carrying a control signal to resolve contention for sending messages to the node E*** (Fig. 3B, page 17, lines 8-20, page 7, lines 1-20), ***the control signal resolving contention at least partly on the basis of QoS*** (the basis of QoS is not defined, therefore, translates into priority of message where a message from a node on the same level has higher priority than a message from a node one level above, page 7, lines 15-20 and page 47, lines 3-6).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 9, 11-14, 43-44, and **50** are rejected under 35 U.S.C. 103(a) as being unpatentable over arts of record, Coke S. Reed (WO 97/04399) in view of Monacos (USPN 5,617,413).

Per **claim 1**, as shown in Fig. 3B, Reed teaches an interconnect structure comprising ***a plurality of interconnected nodes including distinct nodes A*** (A), ***B*** (D), ***C*** (F), ***and D*** (E), ***data interconnect line AB_1, data interconnect line CD_1, a data interconnect line AD, means for detecting a condition at the node C*** (it is inherent that node A is able to detect a condition at the node C (F) following a receipt of control signal sent from node C (F), col. 10, lines 16-22), ***means for sending a control signal CS from the node C*** (F) ***to the node A*** (A) (page 6, lines 24-27 – page 7, lines 1-20, and page 17, lines 8-20), ***the control signal being determined at least in part by the condition at the node C*** (F) (it is inherent that the control signal is determined as to whether the node C (F) having a top priority has a message to send to the node D (E) on the same level, page 7, lines 15-20, page 10, lines 16-22, and page 47, lines 3-6), and ***means for sending a message M arriving at the node A*** (A) ***to the node B***(D) ***or the node D*** (E) ***on a data interconnect line selected from among the data interconnect lines AB_1 and AD depending at least partly on the control signal CS*** (if a message M at the node A (A) is not blocked, i.e. no control signal is sent from the node C (F) indicating that the node C (F) has a message for node D (E), then the message M will be routed to the node D (E) via the line AD connecting the nodes A (A) and the node (E) in Fig. 3B, and if a control signal is received, the message M will be deflected to the node B (D) through the line AB_1 connecting between the nodes A(A) and B (D) in Fig. 3B, page 9, lines 21-26, page 10, lines 16-22, and page 30, lines 14-21).

However, Reed fails to teach data interconnection lines AB_2 and CD_2. As shown in Fig. 6, Monacos teaches the second data interconnection line AB_2 connecting between output port 5 of node A (the claimed node A) and input port 5 of node C (the claimed node B), and the second

data interconnection line CD_2 connecting between output port 5 of node B (the claimed node C) and input port 5 of node D (the claimed node D).

Given the teaching of Monacos, it would have been obvious to one skilled in the art to incorporate the data interconnection lines AB_2 and CD_2 into the structure of Reed to support an increase in bandwidth requirement and/or provide redundancy to the links as known in the art.

Claim 43 is a method claim corresponding to an interconnect structure claim 1, and is rejected under the same reason set forth in the rejection to claim 1 with the additions that (i) the nodes A and B are on the level in the hierarchy and the nodes C and D are on a next level as shown in Fig. 3B, and (ii) lines B_1, B_2, D_1, D_2, and D_3 corresponds to lines AB_1, AB_2, CD_1, CD_2, and AD in claim 1, respectively.

Per **claim 2**, Reed teaches that ***the control signal CS is carried from the node C*** (F) ***to the node A*** (A) ***on a control interconnect line from the node C*** (F) ***to the node A*** (A) (Fig. 3B and page 17, lines 8-11 and 15).

Per **claim 3**, Reed teaches that ***every output port reachable from the node A is reachable from the node C*** (as both nodes A and C are trying transmitting the data to node D, therefore, it is inherent that node D is in a suitable path for accessing a destination device and the output port of the destination device is reachable from both nodes A and C, page 29, lines 25-28, page 30, lines 14-16, page 33, lines 14-17), and ***an output port that is reachable from node A and is not reachable from the node B*** (an output port of a destination device corresponding to a message sent to node A is not reachable from node B, page 22, lines 15-18)

Per **claim 4**, Reed teaches that ***the line AD passes directly from the node A*** (A) ***to the node D*** (E) (Fig. 3B).

Per **claim 5**, Reed fails to teach that the line AD passes through a node between the node A and the node D on the line AD. Monacos teaches ***the line AD passes through a node*** (node E in Fig. 1) ***between the node A*** (A) ***and the node D*** (F) ***on the line AD*** (the line AF is connecting node A to node E, node E to B, and node B to F in Fig. 1).

Per **claim 9**, Reed teaches that ***when the condition at the node C*** (F) ***is that the node C*** (F) ***sends a message on each line from the node C*** (F) ***to the node D*** (E), ***then the node A*** (A) ***can send no messages to the node D*** (E) (when the node C (F) has a message to send to the node D (E), node C (F) has a higher priority than node A (A), Fig. 3B, page 30, lines 14-16 and page 47, lines 3-6).

Per **claim 11**, Reed teaches ***a message M is sent from the node A*** (A) ***through the node D*** (E) ***to its target destination*** (page 29, lines 25- page 31, lines 25-28-page 32, lines 1-2), but fails to teach that the message M is selected from a message set R containing each message at the node A that can reach the target of the message M through the node D.

However, it is well known that there might be more than one message (the message set R) at the node A (A in Fig. 3B) that has the same destination as that of message M and is waiting to be routed through the node D (E in Fig. 3B) to its destination. Therefore, it would have been obvious to one skilled in the art to select the message M from the message set R to be sent from the node A to the node D in a case when the message M, e.g. an ATM cell, has a highest priority in the message set R for QoS purposes (page 4, lines 13-18) and/or arrives at the node A first for FIFO routing purposes as known in the art.

Per **claim 12**, Reed teaches that the interconnect structure can be used in ATM machines (page 4, lines 13-18), therefore, it is inherent that there may be a case where no message in the message set R has a higher level of QoS than the message M.

Per **claim 13**, Reed further teaches that it is also inherent that there may be a case when ***a message in the message set R with the same level of QoS as the message M is not sent to the node D*** (E in Fig. 3B) ***based on information*** (information is not defined, therefore, reads on control signal sent from the node C (F in Fig. 3B) indicating that the node C has a message to send to the node D) ***from the node A*** (page 29, lines 25-28 and page 30, lines 14-16).

Per **claim 14**, Reed teaches that the interconnect structure can be used in ATM machines (page 4, lines 13-18), therefore, it is inherent that messages in the message set R are ATM cells with different QoS levels as known in the art. Reed also teaches different priority levels the messages have based on the node last visited node prior to arrival at the node A (page 42, lines 23-28). However, Reed fails to teach a message selecting means.

It would have been obvious to one skilled in the art to include a message selecting means to automatically select a message at node A from the message set R for sending to node D based on the level of QoS and the node last visited prior to arrival at node A of the messages in the message set R in order to appropriately provide different QoS levels to different messages.

Per **claim 44**, Reed teaches ***sending the message M from the node A*** (node A) ***to the node D*** (node E) ***when the condition at the node C*** (node F) ***is that no messages are moving from the node C to the node D and a path exists from the node D to the target destination of the message M*** (Fig. 3B, page 10, lines 16-19, page 29, lines 25-28).

Per **claim 50**, Reed teaches that the structure can be used with ATM machines (page 4, lines 13-18), therefore, it is inherent the messages in a case of ATM cells must include ***high QoS messages and low QoS messages*** and ***QoS information in the header*** as well known in the art, and ***the messages have a header including information specifying a target destination for ultimately receiving the message*** (page 31, lines 25-page 32, lines 1-2).

Reed fails to teach that the message M is selected from a message set R which contains high QoS messages and low QoS messages.

However, it is well known that there might be more than one message (the message set R) at the node A (A in Fig. 3B). Therefore, it would have been obvious to one skilled in the art to select the message M from the message set R to be sent from the node A to the node D in a case when the message M, e.g. an ATM cell, has a highest priority in the message set R for QoS purposes (page 4, lines 13-18) and/or arrives at the node A first for FIFO routing purposes as known in the art.

Claims 15-18, 21, 26, 37-38, 40-41, 51, and **56** are rejected under 35 U.S.C. 103(a) as being unpatentable over an art of record, Coke S. Reed (WO 97/04399).

Per **claim 15**, as shown in Fig. 3B, Reed teaches an interconnect structure comprising a plurality of nodes including ***distinct nodes A*** (A), ***C*** (F), ***and D*** (E), ***a plurality of interconnect lines coupling the nodes, the node D*** (E) ***having one message input interconnect line coupled to the node A*** (A) ***and one message interconnect line coupled to the node C*** (F) (page 17, lines 8-20), ***a logic that enforces priority relationship rules*** (page 33, lines 6-12) ***including rules for governing the sending of messages from the nodes A (A) and C (F) to the node D*** (E) ***so that for a message MA arriving at node A*** (A) ***and a message MC arriving at node C*** (F), ***the***

message MC is not blocked from traveling to node D (E) ***by the message MA*** (page 29, lines 25-28 and page 47, lines 3-6).

Although Reed does not teach rules governing the sending of messages from the node A to the node D depending at least in part on QoS levels of messages at node A, Reed further teaches that the structure can be used in ATM machines (page 4, lines 13-18), therefore, it is inherent that the messages at node A can be ATM cells each with different QoS levels.

Therefore, it would have been obvious to one skilled in the art to incorporate rules governing the sending of messages, e.g. ATM cells, from the node A to the node D depending at least in part on QoS levels of messages at node A to appropriately accommodate different QoS levels into the claimed logic so that different QoS can also be automatically enforced as priority relationship rules in the system.

Per **claim 37**, Reed teaches an interconnect apparatus, comprising ***a plurality of nodes*** (page 4, lines 21-27), ***a plurality of interconnect lines selectively coupling the nodes in a hierarchical multiple level structure*** (page 4, lines 21-27 and page 5, lines 19-20), ***the level of a node being determined entirely by its position in the structure*** (page 6, lines 24-27, and page 7, lines 21-page 8, lines 1-7) ***in which data moves unilaterally from a source level to a destination level or laterally along a level of the multiple level structure*** (page 9, lines 21-26) , ***a plurality of data messages being transmitted through the structure from a source node*** (a node at level J) ***to a designated destination node*** (a node at level zero) (page 4, lines 27-28, page 10, lines 10-13), ***a level of multiple levels includes one or more groups of nodes*** (page 4, lines 24-26), ***the data messages being transmitted to a group of the one or more groups of nodes on a path to a target*** (page 9, lines 17-26), ***a group of the one or more groups including a plurality of nodes***

(nodes at lower levels on a path toward the destination level zero, e.g. nodes F and E in Fig. 3B), ***a single data message*** (message M) ***being transmitted to a node N*** (node E in Fig. 3B) ***of the plurality of nodes of a group unilaterally toward the destination level if the node*** (node E in Fig. 3B) ***is not blocked and otherwise one or more data messages being transmitted laterally if the node is blocked*** (page 9, lines 21-26).

Although Reed fails to teach that the data messages being transmitted based at least partly on QoS of the messages, Reed also teaches that the structure can be used with ATM machines (page 4, lines 13-18), therefore, it is inherent the messages (e.g. ATM cells) include high QoS messages and low QoS messages as well known in the art.

Therefore, it would have been obvious to one skilled in the art to incorporate transmitting the data messages, e.g. ATM cells, based partly on QoS of the messages in order to appropriately accommodate messages with different QoS levels.

Per **claim 38**, Reed teaches a network comprising ***a plurality of nodes*** (page 4, lines 21-24), ***the nodes includes communication devices*** (e.g. ATM machines) ***that receive messages and send messages*** (page 4, lines 13-18 and 28-29), ***the message includes high QoS messages*** (e.g. ATM cells with CBR QoS as known in the art) ***and low QoS messages*** (ATM cells with UBR QoS as known in the art) (it is inherent that messages M must include ATM cells with different QoS when ATM machines are used in the network, page 4, lines 13-18), ***a plurality of interconnect lines L interconnecting communication devices at the plurality of nodes*** (ATM machines at the respective nodes) (page 4, lines 21-24, Fig. 3B and page 17, lines 8-20), ***a node N*** (E in Fig. 3B) ***of the plurality of nodes includes a connection to one interconnect line L_{UN}*** (a solid line connecting node F to node E in Fig. 3B) ***capable of transmitting a plurality of***

messages from a device U (reads on an ATM machine residing at node F in Fig. 3B, page 4, lines 13-18) ***to the node N (E in Fig. 3B), a connection to an interconnect line L_{VN}*** (a solid line connecting node A to node E in Fig. 3B) ***for transmitting a message from a device V*** (reads on an ATM machine residing at node A in Fig. 3B, page 4, lines 13-18) ***to the node N*** (E in Fig. 3B), ***the network having a precedence relationship P_N (U,V) relating to the node N and the devices U and V*** (if at time step t (zero) both nodes F and A has a message (M_U and M_V, respectively) to send to node E, then node F which has higher priority than node A will get to send a message (M_U) to node E, Fig. 3B, page 30, lines 13-20 and page 47, lines 3-6), ***and the node V uses a control signal*** (sent by node F in Fig. 3B) ***to decide where to send the message M_V*** (page 9, lines 21-26 and page 30, lines 13-21).

However, Reed does not teach determining the precedence relationship P_N (U,V) at least partly by QoS of the messages.

It would have been obvious to one skilled in the art to determine the precedence relationship P_N (U,V) at least partly by QoS of the messages to appropriately accommodate the messages (ATM cells) with different QoS levels, for example ATM cells with CBR QoS will be transmitted before ATM cells with UBR QoS to meet a delay requirement as known in the art.

Per **claim 40**, Reed teaches a network capable of carrying ***a plurality of messages M concurrently*** (more than one message data is being carried in the network, page 5, lines 1-3), ***the messages including high QoS messages*** (ATM cells with CBR QoS) ***and low QoS messages*** (e.g. ATM cells with UBR QoS) (it is inherent that messages M must include ATM cells with different QoS when ATM machines are used in the network, page 4, lines 13-18), ***a plurality of output ports P*** (output ports of devices connected to but reside outside the interconnect structure,

i.e. devices E and F, page 5, lines 3-7), ***a plurality of nodes N*** (page 4, lines 21-27), ***the individual nodes N including a plurality of direct message input interconnections and a plurality of direct message output interconnections*** (page 4, lines 28-page 5, lines 1, and page 17, lines 8-20 and Fig. 3B), ***the individual nodes N for passing messages M to predetermined output ports*** (designated output ports of destination devices) ***of the plurality of output ports P and the predetermined output ports P being designated by the messages M*** (page31, lines 25-page 32, lines 1-2 and page 4, lines 27-28), ***a plurality of interconnect lines in an interconnect structure selectively coupling the nodes in a hierarchical multiple level structure arranged to include a plurality of J+1 levels in an hierarchy of levels arranged from a lowest destination level L_0 to a highest level L_J which is farthest from the lowest destination level L_0*** (page 4, lines 21-27 and page 5, lines 19-20), ***the output ports P being connected to nodes at the lowest destination level L_0*** (output ports of destination devices are connected to nodes on a level zero, page 4, lines 27-28 and page 5, lines 3-6, see also page 31, lines 25-page 32, lines 1-2), ***the level of a node being determined entirely by its position in the structure*** (page 6, lines 24-27, and page 7, lines 21-page 8, lines 1-7), ***the network includes a node A*** (node A, page 5, lines 10-18), ***a control signal operating to limit the number of messages that is allowed to be sent to the node A to eliminate contention for the predetermined output ports of the node A*** (node A sends a control signal to a device G to indicate whether node A is ready to receive message data from a device G, page 7, lines 16-18, see ~~also page 7,~~ lines 10-13) ***so that the messages M are sent through the direct message output connections of the node A to nodes H*** (nodes at lower level on the path toward the destination level) ***that are a level L no higher than the level of the node***

A, the nodes H being on a path to the designated predetermined output ports P of the messages M (page 9, lines 21-26, page 22, lines 11-12, 15-18, and page 31, lines 25-page 32, lines 1-2).

Although Reed fails to teach that the control signal being determined at least partly according to message QoS, it would have been obvious to one skilled in the art to use message QoS to determine the control signal in order to appropriately provide messages with different QoS levels, for example if node A is transmitting a message data with CBR QoS with high priority, then the control signal may be sent from node A to a device G informing that it is not ready to receive another message data from the device G.

Per **claim 41**, Reed teaches an interconnect apparatus comprising ***a plurality of nodes and a plurality of interconnect lines*** (page 4, lines 21-24), ***a plurality of J+1 levels in an hierarchy of levels arranged from a lowest destination level L_0 to a highest level L_J*** (page 24, lines 24-28 and page 5, lines 19-20), ***the level of a node being determined entirely by its position*** (page 6, lines 24-27, and page 7, lines 21-page 8, lines 1-7), ***the interconnect structure transmitting a plurality of multiple-bit messages entering the interconnect structure unsorted through a plurality of input ports*** (input ports of nodes at level J) (page 5, line 10, page 22, lines 11-12, 15-18, page 31, lines 25-page 32, lines 1-2), ***individual messages M being self-routing*** (having header designating the target ring in a binary form, page 31, lines 25-page 32, lines 1-2) and ***including high QoS messages*** (ATM cells with CBR QoS) ***and low QoS messages*** (e.g. ATM cells with UBR QoS) (it is inherent that messages M must include ATM cells with different QoS when ATM machines are used in the network, page 4, lines 13-18), ***message M exits an output port designated by the message M*** (page 31, lines 25-page 32, lines 1-2) ***using the three ways being (1) the message M enters a node*** (a node A) ***in the interconnect structure***

from an external device (a device C) (page 5, lines 10-14), ***the message M designating one designated output port*** (page 31, lines 25-page 32, lines 1-2), ***(2) the message M moves through a node to a designated output port, a time T being associated with the node such that the message M arriving at the node is selectively transmitted within the time T of the message's arrival at the node*** (page 31, lines 22-25, page 32, lines 3-page 33, lines 5), ***(3) the message M moves either (i) through a node U*** (node N(r,θ, z) = N(T,θ, z)) ***on a level L_k*** (level r, where r = T) ***to a different node V*** (node N(T,θ+1,h_T(z)) ***on the same level L_k in combination with another message, if available, or (ii) moves through the node U on a level L_k to a node*** W (node N(T-1, θ+1,z)) ***on a level L_i*** (T-1) ***nearer in the hierarchy to the destination level L_0 than the level L_k*** (page 33, lines 6-26), ***a time T_U being associated with the node U such that the message M arriving at the node U is selectively transmitted within the time TU of the message M arrival at the node U*** (page 31, lines 22-25, page 32, lines 3-22, and page 33, lines 6-26).

Although Reed fails to teach that movement of the message M is determined by QoS of the message M, it would have been obvious to one skilled in the art to utilize QoS of the message M to determine movement of the message M in order to provide appropriate QoS level to the message M.

Per **claim 51**, Reed teaches an interconnect structure comprising ***a collection of nodes*** (page 4, lines 21-24) ***including distinct nodes A, B, C, and D*** (nodes A, D, F and E as shown in Fig. 3B, respectively), ***a collection of interconnect lines selectively coupling the nodes of the interconnect structure*** (page 4, lines 21-24, page 17, lines 8-20, and Fig. 3B), ***a logic for routing packets through the interconnect structure so that the node A is capable of sending packets to the node B or the node D*** (page 33, lines 6-25 and Fig. 3B), ***for a packet PA arriving at the***

node A and a packet PC arriving at the node C, the node C has routing priority over the node A to send messages to the node D in which routing of the packet PA at the node A depends upon routing of the packet PC at the node C (Fig. 3B, page 29, lines 25-28, page 30, lines 14-21, and page 47, lines 3-6).

Although Reed fails to teach routing of the packet PC at the node C depends at least partly on a QoS of service of the packet PC, Reed further teaches that ATM machines can be used in the interconnect structure, therefore, it is inherent that packets are in the form of ATM cells with different QoS levels, e.g. CBR with high QoS or UBR with low QoS as known in the art (page 4, lines 13-18).

Therefore, it would have been obvious to one skilled in the art to route the packet PC at the node C based partly on a QoS of service of the packet PC to ensure the QoS of the packet PC.

Per **claim 56**, Reed teaches an interconnect structure comprising ***a plurality of nodes*** (page 4, lines 21-24) ***including the distinct nodes A, B, C, and D*** (nodes A, D, F and E as shown in Fig. 3B, respectively), ***a collection of interconnect lines selectively coupling the nodes of the interconnect structure*** (page 4, lines 21-24, page 17, lines 8-20, and Fig. 3B), ***including one*** (one) ***or more data carrying lines allowing the node A to send messages to the node B, one*** (one) ***or more data carrying lines allowing the node A to send data to the node D, and one*** (one) ***or more data carrying lines allowing for the node C to send data to the node D*** (Fig. 3B and page 17, lines 8-20), and ***a logic for routing packets through the interconnect structure so that a message M_C arriving at the node C is not blocked from being routed to the node D by a message M_A arriving at the node A*** (page 33, lines 6-26, page 29, lines 25-28, page 30, lines 14-

21, and page 47, lines 3-6), ***messages arriving at the node A are routed by a logic associated with the node A to other nodes in the interconnect structure*** (page 33, lines 6-26).

Although Reed fails to teach that the logic at node A uses QoS information from the messages arriving at node A at least in part to route the messages to other nodes in the interconnect structure, Reed further teaches that that ATM machines can be used in the interconnect structure, therefore, it is inherent that messages are in the form of ATM cells with different QoS levels, e.g. CBR with high QoS or UBR with low QoS as known in the art (page 4, lines 13-18).

Therefore, it would have been obvious to one skilled in the art to modify the logic so that the logic will use QoS information from the messages arriving at node A at least in part to route the messages to other nodes in the structure to ensure the QoS of the messages.

Per **claim 16**, Reed teaches that ***the rules governing the sending of messages from the node A to the node D depend in part on the number*** (the number is not defined, therefore, reads on one (1)) of ***messages that the node C sends to the node D*** (node A will be blocked from transmitting the message to node D if node C has a message to transmit to node D, page 29, lines 25-28 and page 30, lines 14-16).

Per **claim 17**, Reed teaches that ***the rules governing the sending of messages from the node A to the node D depend at least in part on routing by the node D of message arriving at a node subsequent to the node D*** (messages are routed from node A (N) to node D (N') if the messages' destination is accessible from node D (N'), page 10, lines 16-19).

Per **claim 18**, Reed teaches that ***wherein one or more messages N exist so that when the node C sends a message N to the node D, then the node A is not allowed to send messages to***

the node D (when node C (F in Fig. 3B) which has a higher priority has a message to send to node D (E in Fig. 3B), node A cannot send message to node D, page 29, lines 25-28 and page 30, lines 14-16).

Per **claim 21**, Reed teaches that ***the rules specify that when the node C sends no messages to the node D then the node A sends a message from the node A to the node D so long as a message M is present at the node A and a path exists from the node D to a target of the message M*** (page 10, lines 16-19 and page 29, lines 25-28).

Per **claim 26**, Reed teaches that ***the rules specify that when the node C sends two messages to the node D, then no message is sent from the node A to the node D*** (it is inherent that as long the node C has messages with higher priority to send, then node A (N or A in Fig. 3B) cannot sent a message to node D (N' or E in Fig. 3B), page 10, lines 16-19 and page 30, lines 14-16).

Allowable Subject Matter

6. (i) Claims 6-8, 10, 19-20, 22-25, 28, 30-36, 45-49, 52-55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(ii) Claims 27 and 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

(iii) Claim 39 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action. The cited prior arts alone

or in combination fail to teach or make obvious on the following when considered in combination with other limitations in the claim: the messages M and control signal C being received by a node of the plurality of nodes at a discrete time step t.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nittaya Juntima whose telephone number is 703-306-4821. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 703-308-5340. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-9408 for regular communications and 703-827-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Nittaya Juntima
June 17, 2003
NJ

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600